

The new standard for low-power Wi-Fi.

Every Wi-Fi front-end on the market is a non-linear amplifier with a correction engine bolted on. It works — until the channel gets wide, the battery gets small and the traffic gets bursty. **Elementum™ is linear by design.** One chip, in standard 300 mm silicon, clean on the first symbol of every burst, at power. It drops into the socket you already have.

0.15 nJ

per bit delivered

320 MHz, low-power mode, third-party measured

1.7×

the output power

at the signal quality competitors publish

2.0×

cleaner signal

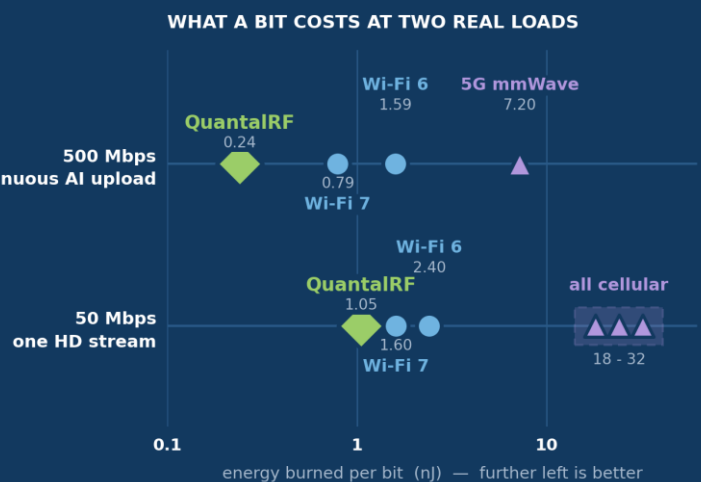
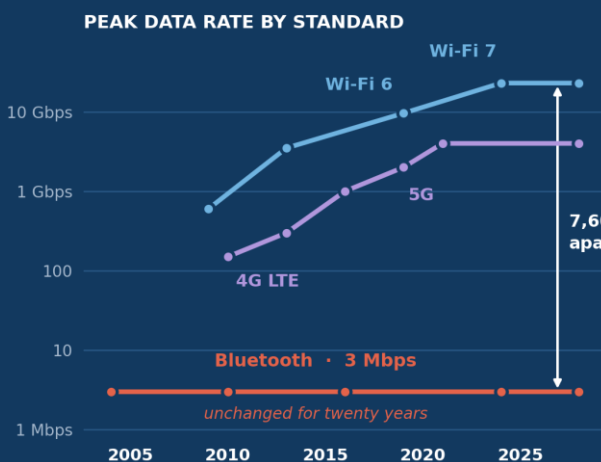
at the output power competitors publish

5.2×

more output power, on average

across all conditions and use cases, vs incumbent Wi-Fi front-ends

DATA RATES RAN AWAY. THE ENERGY TO MOVE THEM DID NOT.



Energy per bit = transmit energy plus link-maintenance power divided by offered load (cellular 0.60 W, Wi-Fi 0.045 W — the same overhead applied to Elementum™ as to Wi-Fi 7). The Elementum™ figure is third-party measured; the others are estimated from published module power and throughput.

At the load an AI product actually creates, Elementum™ moves a bit for **0.15 nJ** against the **0.6 nJ** a mainstream Wi-Fi front-end spends — 3.7× less energy, and a thirtieth of what 5G spends — and fits a wearable battery while doing it.

WHERE ELEMENTUM™ GOES

Mobile phones

Access points

AI-edge wearables

AI glasses & XR

Cameras & NVR

Robots & drones

Range stops being a power problem. Battery life stops being a heat problem. Bandwidth stops being a noise problem. **You do not improve wireless — you change what a product can be.**

A DROP-IN, NOT A REDESIGN

Pin-to-pin compatible

Same footprint, same control interface, **fully mode compliant**. It lands in the socket you already routed.

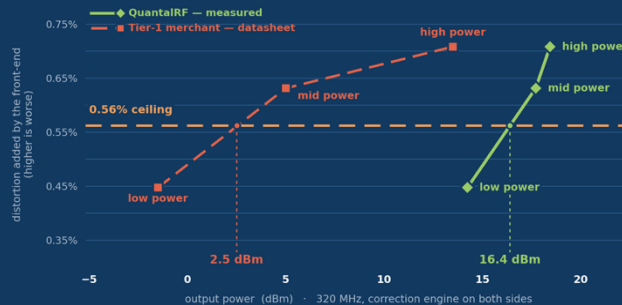
No software changes

Same power modes, same gain states, same calibration flow. **No driver work, no re-tuning, no new firmware.**

Margin, not risk

A straight swap works at **16 of 16** settings — their mode, power, channel and data rate — arriving **3× to 16× cleaner** than that socket needs.

CLEAN AT POWER — THE WHOLE ARGUMENT IN ONE CHART



At 320 MHz a tier-1 merchant front-end crosses the 0.56% ceiling at 2.5 dBm; Elementum™ crosses it at 16.4 dBm — mode for mode, at identical distortion, **3× the power in high power, 19× in mid, 37× in low**. Merchant figures are published datasheet values; ours are measured.

ONE CHIP. STANDARD SILICON. 300 MM.

Single chip, 130 nm RF SOI

PA, LNA, switch and control on **one die** of **1.9 mm²** — not a GaAs PA bonded to a silicon controller in a multi-die module.

300 mm, not 150 mm

Four times the area per wafer on a smaller die, in **mainstream foundry and OSAT capacity** — not specialty compound lines.

It travels with you

Proven path from 130 nm SOI to **40 nm**, and from silicon to **GaAs and GaN**. Energy per bit falls from **0.15 nJ today to 0.032 nJ by 2030**, at the same speed and output power.

WHAT IT CHANGES IN THE PRODUCT

Moving **10 GB** off a pair of AI glasses goes from **111 seconds to 28**, and from **32 J to 15 J**. And the correction engine leaves your bill of materials: a DPD datapath, observation receiver, gigasample ADC and adaptation solver cost **150–350 mW per transmit chain, 5–12% of SoC die area** and roughly **\$0.10–0.30 per chip** — on every chain.

AVAILABILITY AND SUPPLY

Now

samples and evaluation kits

available today, with platform enablement support

Q1 2027

volume production

JEDEC JESD47 qualified, ten-million-unit production run

300 mm

GlobalFoundries and ASE

mainstream foundry and assembly, capacity allocated

< 10 ppm

defect rate at volume

the level a tier-1 account accepts

KEY SPECIFICATIONS — QWX27104

Standards and band	Wi-Fi 7 and Wi-Fi 8 compatible, full 5150–7125 MHz range
Linear output power	23 dBm at HE20 MCS0, with 3 dB spectral-emission-mask margin
Wideband performance	Specified < -46 dB EVM to 16 dBm at 320 MHz; third-party measured better than -44 dB to 18 dB . Mask-limited out to 19.5 dBm
EVM consistency	< 0.5 dB across every channel , against more than 4 dB for competitive GaAs front-ends
DPD and mismatch	Low-order engine only, offloading the host SoC; EVM held under 3:1 VSWR
Supplies and package	3.8 V PA, 1.8 V LNA · 2 × 2 mm 16-pin LGA, or under 2 mm² flip-chip die